



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/082,663	05/21/1998	RICHARD L. SOLOMON	97125	2987

24319 7590 09/23/2004

LSI LOGIC CORPORATION
1621 BARBER LANE
MS: D-106 LEGAL
MILPITAS, CA 95035

EXAMINER

PHAN, THAI Q

ART UNIT

PAPER NUMBER

2128

DATE MAILED: 09/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/082,663	Applicant(s) SOLOMON, RICHARD L.	
	Examiner Thai Q. Phan	Art Unit 2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 21 June 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-45 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 27-34 is/are allowed.
- 6) ☒ Claim(s) 1-26 and 35-45 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date: _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date: _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This Office Action is in response to applicant's amendment filed on 6/21/2004.

Claims 1-45 are pending in the Action.

Claim Rejections - 35 USC § 112

Due to applicant's amendment to the claims, the 35 USC 112 claim rejection has been withdrawn.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-26 and 35-45 are rejected under 35 U.S.C. 102(e) as being anticipated by Pearce et al, US patent no. 5,796,984.

As per claim 1, Pearce anticipates a method and system for emulating peripheral device functions and even eliminating device functions (or peripheral device disconnected from a bus) with feature limitation very similar to the claimed invention (Abstract and Field of the Invention). According to Pearce, the method includes steps

Art Unit: 2128

detecting a signal on the bus indicating a request to access the peripheral device (col. 4, lines 8-17),

monitoring the bus for a response by the peripheral device (col. 3, lines 18-45, col. 6, lines 61 to col. 7, line 13, Figs. 3 and 5), and

sending an emulated or mimicked response to the signal when a selected period of time passes without a response being made by the peripheral device (col. 8, lines 47-67, col. 9, lines 1-15, lines 25-42, lines 55-62, for example).

As per claim 2, Pearce anticipates a bus interface including small computer system bus interface (col. 5, lines 1-13, lines 37-48, for example).

As per claim 3, Pearce discloses sending a first signal that indicates a presence of the device being emulated on the bus (Figs. 3, 5, col. 6, line 61 to col. 7, line 13, for example).

As per claim 4, Pearce discloses bus interface with bus busy signals.

As per claim 5, Pearce anticipates step of sending a signal in response to the request (col. 6, lines 33-39).

As per claim 6, Pearce discloses sending not ready signal for device access and retrieval information.

As per claim 7, Pearce discloses a preselected data sequence in the second signal in peripheral device emulation (col. 5, lines 1-20).

As per claims 8 and 10, Pearce anticipates the limitations for other peripheral bus devices to emulate the peripheral device functions as claimed.

As per claim 9, Pearce discloses the peripheral device emulated and processing peripheral device emulation to eliminate the peripheral device presence (Figs. 3, 5, and 9).

As per claims 11 and 12, Pearce anticipates a preset response in the memory access from the bus device, and responses made by the peripheral device when the device is present or eliminated on the bus (col. 8, line 15 to col. 10, line 30).

As per claim 13, Pearce disclosure require a state machine implemented in the bus device for implementing process of monitoring, detecting, and sending responses as claimed (Figs. 5, col. 7, lines 14-31, col. 8, lines 15-36, for example).

As per claim 14, Pearce anticipates a method and system for emulating peripheral device functions and even eliminating device functions (or peripheral device disconnected from a bus) with feature limitation very similar to the claimed invention (Abstract and Field of the Invention). According to Pearce, the method includes steps

detecting a signal on the bus indicating a request to access the device (col. 4, lines 8-17),

monitoring the bus for a response by the device (col. 3, lines 18-45, col. 6, lines 61 to col. 7, line 13, Figs. 3 and 5), and

sending an emulated or mimicked response to the signal after a selected period of time passes without a response being made by the peripheral device, wherein the emulated or mimicked response indicates to the operating system that the peripheral device is present within the data processing system (col. 8, lines 47-67, col. 9, lines 1-15, lines 25-42, lines 55-62, for example).

Art Unit: 2128

As per claim 15, Pearce anticipates bus and computer system interface bus as claimed (Figs. 3-5).

As per claim 16, Pearce discloses sending a response including a signal that indicates a presence of the device being emulated on the bus (cols. 6-8).

As per claim 17, Pearce discloses bus signals which including bus busy signals .

As per claim 18, Pearce anticipates a data processing system for emulation of present of the peripheral device in the system bus with feature limitations similar to the claimed invention. According to Pearce, the system includes

a bus (Figs. 1-3),

means for detecting a signal on the bus indicating a request to access the peripheral device (cols. 4-6),

means for monitoring the bus for a response by the peripheral device (col. 3, lines 18-45), and

means for sending a response to the signal within bus cycles intended without a response being made by the peripheral device as claimed.

As per claim 19, Pearce anticipates system bus and bus interface to the system as claimed.

As per claim 20, Pearce anticipates means for sending signal the system operating system to indicate a presence of the device on the bus (cols. 6-8).

As per claims 21-26, Pearce anticipates bus signals as claimed for accessing to the peripheral device (Figs. 3-5, cols. 6-8).

As per claim 35, claims 35 is directed to a computer program product for use with a data processing system for emulating a device for controlling and processing method as in claim 1 above and Pearce anticipates a method and system for emulating peripheral device functions and even eliminating device functions (or peripheral device disconnected from a bus) with feature limitation very similar to the claimed invention (Abstract and Field of the Invention). According to Pearce, the computer program medium includes program means for

detecting a signal on the bus indicating a request to access the peripheral device (col. 4, lines 8-17),

monitoring the bus for a response by the peripheral device (col. 3, lines 18-45, col. 6, lines 61 to col. 7, line 13, Figs. 3 and 5), and

sending an emulated or mimicked response to the signal when a selected period of time passes without a response being made by the peripheral device (col. 8, lines 47-67, col. 9, lines 1-15, lines 25-42, lines 55-62, for example).

As per claims 36-40, Pearce discloses bus signals as claimed in bus access operations.

As per claims 41, Pearce anticipates a method and system for emulating peripheral device functions and even eliminating device functions (or peripheral device disconnected from a bus) with feature limitation very similar to the claimed invention (Abstract and Field of the Invention). According to Pearce, the method includes steps

detecting a signal on the bus indicating a request to access the device (col. 4, lines 8-17),

monitoring the bus for a response by the device (col. 3, lines 18-45, col. 6, lines 61 to col. 7, line 13, Figs. 3 and 5),

emulating the peripheral device or ascertaining that the peripheral device being requested is to be mimicked or emulated, and

sending an emulated or mimicked response to the signal when a selected period of time passes without a response being made by the peripheral device (col. 8, lines 47-67, col. 9, lines 1-15, lines 25-42, lines 55-62, for example).

As per claim 42, Pearce discloses emulated or mimicked response includes pre-stored data according to a bus protocol (Figs. 3-5, col. 6, col. 9, lines 43-62).

As per claim 43, Pearce discloses starting a timer for emulation of the peripheral device by CPU 305 and SMM (Fig. 4, 5, col. 10, line 55 to col. 11, line 30).

As per claims 44, Pearce discloses the claimed limitations for peripheral device emulation as claimed.

As per claim 45, Pearce discloses bus access including bus release as claimed.

Allowable Subject Matter

Claims 27-34 are allowed. The following is a statement of reasons for the indication of allowable subject matter:

Claims 27-34 are directed to an emulation device within a data processing system for emulating a selected peripheral device within the data processing system. The device emulation includes a mimic device connected to the SCSI system bus interface, wherein the mimic device monitors the bus for a signal selecting a selected

Art Unit: 2128

device within the plurality of peripheral devices for an input and output transaction during initialization of an operating system within the data processing system, monitors the bus for a response by the selected device in response to detecting the signal, selecting the device, and sends a response to the signal a selected period of time passes without a response being made by the selected device, wherein the response indicates to the operating system that the selected device is present within the data processing system.

Because the closest prior art in the record does not expressly disclose the emulation device connected to the SCSI bus of the data processing system with feature limitations as above, thus the mimic device for peripheral device emulation allows a peripheral device to be disconnected from the bus, while requests may be still be directed to the peripheral device for reducing the time associated with a device swap and to reduce the disruption to users of a data processing system, claims 27-34 are thus deemed allowable.

Response to Arguments

Applicant's arguments with respect to features in the amended claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

1. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thai Q. Phan whose telephone number is 703-305-3812.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean Homere can be reached on 703-308-6647. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2128

3. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sept. 15, 2004



Thai Phan
Patent Examiner
Art Unit 2128